International Journal of Global Engineering (IJGE) E- ISSN: 2456-3099

VOL 1 ISSUE 4 (2017) PAGES 1 - 5

Received: 28/03/2017. Published: 26/04/2017

ENERGY EFFICIENT FREQUENCY MULTIPLIER FOR SILICON ON CHIP

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ABSTRACT:

Now a days the digital signal processing and its classification applications on the energy constrained devices should be supported on the basis of efficiency. Because such applications have to perform highly complex computations especially complex multiplication processes while exhibiting tolerance for a large amount of noise and for computational errors too. So, comparing all the arithmetic computations, improving the energy efficiency of multiplication is critical. In this brief, an energy efficient approximate m bit vedic multiplier is proposed which gives a trade off between computational accuracy and energy consumption. The proposed architecture has reduced area compared to other multiplier architectures which process same number of bits. The reduced architecture area reduces the power consumption. Also the vedic technology adopted for the multiplication reduces the delay further. But the approximate architecture output possess a small amount of computational accuracy which is negligible for DSP applications. .

Keywords: digital signal processing; energy efficient; vedic multiplier; approximate multiplier.

1. INTRODUCTION

For today‟s embedded system and mobiles energy consumption is a critical design problem. A lot of efforts have already taken at various levels for improving energy efficiency. Among other arithmetic operations, multiplication is the most time and power consuming operation. It becomes more significant for large operands and complex multiplication. Usually in computing devices for executing the DSP applications and its classifications with more efficiency specialized processors are used. Also many DSP and classification applications are designed to process information which contains large amount of noise. An adaptive pseudo-carry compensation truncation scheme known as PCT scheme is introduced in earlier efforts [4]. On comparing other truncation methods this method yields low error. But the leakage and dynamic power of PCT multipliers are more than other truncated multipliers. Later a novel architecture of multiplier with tunable error characteristics is proposed [5]. The main advantage of the method is that the architecture consumes comparatively less dynamic power. This multiplier is inherently faster and it needs less gate sizing to meet rising frequency constraints. But the drawback of the architecture is that the error rate is a bit high. Then another multiplier called iterative logarithmic multiplier is introduced [6] which uses logarithmic number system. The method follows the Michelle‟s algorithm to an extent but it it doesn‟t follow the approximation techniques. The iterative logarithmic multiplier can afford many number of

correction terms as the error rate reduces with increase in number of correction terms but it increases the power consumption.

In this brief, a new approximate multiplier is proposed which selects consecutive „m" bits from „n" bits of operands. This new method can provide much more energy efficiency than the truncated methods. The error rate is low because it effectively captures the noteworthy lower bits. For DSP and its classification algorithm, generally one of two operands in the multiplication is stored in the memory. Here it is exploited to improve the energy efficiency of the approximate multiplier further. The area can be effectively reduced by the proposed approximate multiplier because a large number of adders and gates can be excluded in this method compared to other multipliers with the actual n bit operands. Within the approximate multiplier architecture a Vedic technology is used for the multiplication which reduces the delay in the multiplication process.

2. LITERATURE SURVEY

R. Hegde and N. R. Shan hag in 1999 proposed a framework for energy efficient digital signal processing [1]. Here to match the critical path delay with the throughput the supply voltage is scaled beyond the critical voltage. To avoid the degradation in the algorithmic performance, algorithmic noise-tolerance (ANT) scheme is applied. Due to deep submicron (DSM) noise the proposed technology can be used to improve the performance of DSP algorithms in presence of bit-error rates of up to 10 -3. In 2002

D. Menard, D. Chillet, C. Charot, and O. Sentieys presented an Automatic floating point to fixed-point conversion for DSP code generation [2] which was a new methodology of implementation in Digital Signal Processors (DSP) under accuracy constraint. This architecture was meant for the minimization of power consumption, time and cost. The methodology defined the optimal fixed point data formats for minimizing the power consumption.

V. K. Chippa, D. Mohapatra, A. Raghunathan, K. Roy, and S. T. Chakradhar proposed a scalable effort hardware design [3] in 2010 as a new approach to tap the reservoir of algorithmic resilience and translate it into highly efficient hardware implementations. at each level of design abstraction the scalable effort design approach identifies mechanisms that can be used to vary the computational effort expended towards generation of the correct result. These scaling mechanisms can be used to achieve improved energy efficiency.

C. H. Chang and R. K. Satzoda in 2010 proposed a low error and high performance multiplexer-based truncated multiplier which uses an adaptive pseudo-carry compensation truncation (PCT) scheme [4]. Among the other existing truncation methods the proposed method gives low average error. The proposed PCT multiplier runs 21% faster than the VCT multiplier with comparable dynamic power dissipation.

3. PROPOSED ARCHITECTURE

Open-loop PLL-based TX achieves high data rates, but its trans- mission quality is affected by the increased close-in phase noise of voltage-controlled oscillator (VCO), frequency drift due to pressure,

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volume, and temperature (PVT) variations and disturbances in VCO control line during modulation, and other nonideal effects. In this brief, we exploit the higher transition frequency (90 GHz, 130 nm) and improved matching performance (for the same device area, W*L) [11] offered by the deep submicrometer devices and demonstrate a static logic gate-based frequency multiplier design for low-power frequency synthesis. The presented digital edge combiner (EC) offers broadband operation with rail-to-rail output swing, low-power, and low-area implementation advantages. The power and area advantages of the proposed digital frequency mul- tiplier comes with a tradeoff in the spectral purity of the generated RF carrier, which is acceptable in the low-power and short-range wireless communication standards. To enhance the lock time, which is an important design parameter in the clock generator, a dual- edge-triggered phase-detector-based DLL core is adopted. Similar to pre- vious frequency multipliers, the proposed

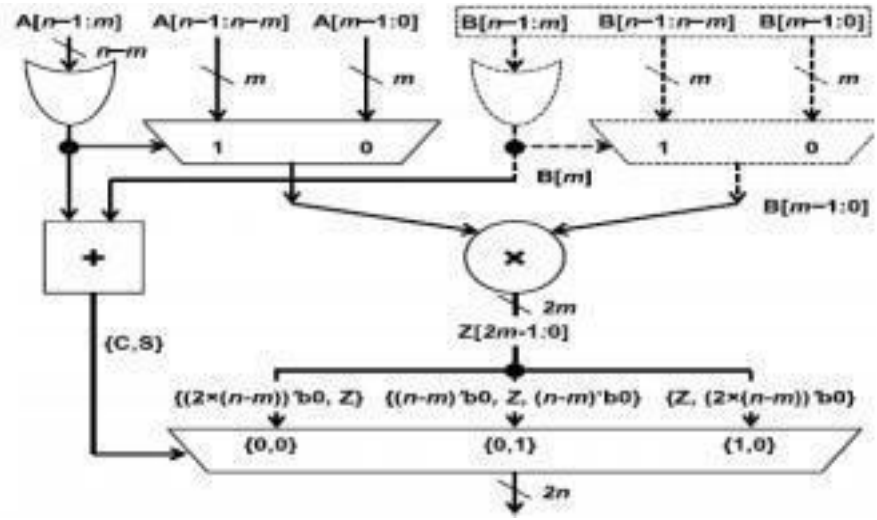

Fig.1. Proposed Architecture

frequency multiplier is also composed of a pulse generator, a multiplication-ratio control logic, and an edge combiner. ratio control signal. Finally, the high-speed and highly reliable edge combiner (HSHR-EC) generates one multiplied clock (CLKMUL) using all the outputs of the multiplication- ratio control logic. Since the number of multiphase is 32, the maximum multiplication ratio is 16. HSHR-EC. As the number of signals merged in the precombining stage (NPRE) increases, the number of PU-Ps and PD-Ns required in the push–pull stage are reduced by a factor of NPRE. It might appear that, by increasing NPRE, the maximum multiplied clock frequency of the HSHR-EC can be enhanced; however, because the logic depth and the number of NAND and NOR gates in the precombing stage are equal to log2NPRE and 32(1– 1/NPRE), respectively, a large NPRE causes the precombining stage to be vulnerable to process variation, which in turn could cause a large deterministic jitter.

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4. RESULT ANALYSIS

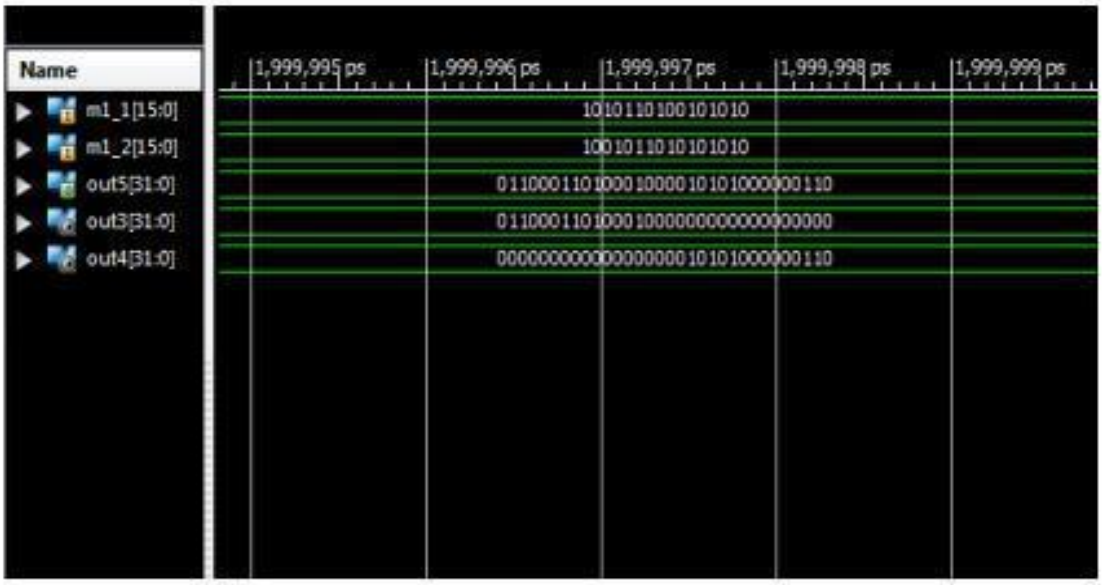

Fig.2. Simulation Analysis

Here the multiplier output is is approximated to 2n bits by suitable shift operations and is mainly meant for DSP applications. Hence the bit error at the approximate output is not much significant. Even though the difference in the approximate output is not much important for DSP applications it can be furthermore improved by steering the m segments from the other set of operands to the multiplier (which is not the output of m bit selection mux). Then this 2n bit output from the output mux is added with the previous 2n bit outputs. The maximum multiplied clock frequency of the proposed frequency multiplier is compared with the previous frequency multipliers. Because it is determined by the edge-combiner structure, he normalized channel widths of the PU-P and the output buffer with respect to the channel width of the PD-N, fMUL,MAX is the maximum multiplied clock frequency, and ERRDUTY is the duty-cycle error of the multiplied clock. However, because the precombining stage in the HSHR-EC merges two signals into one, the self-loading of the push–pull stage (output loading of the push–pull stage except the loading induced by the output buffer) is halved. The frequency multiplier in has the best performance among the previous with frequency multiplier architectures. However, the normalized area of the proposed clock generator, which is the area divided by the product of the square of the process technology and the maximum multiplication ratio, is lower than that of other clock generators. where MRMAX is the maximum multiplication factor. Compared with DLL with frequency multiplier architectures, the proposed clock generator shows the superior performance according to both FoM1 and FoM2, as expected. Note that both the multiplying DLL and the PLL architecture in [18] show superior performance than the proposed clock generator in FoM1. Even the area and the multiplication ratio are considered using FoM2, the multiplying

DLL in is still shows better performance than the proposed clock generator. This result is mainly due to the outstanding power consumption of the multiplying DLL and the PLL architecture.

CONCLUSION

Area, power consumption and increased delay are the constituent factors in VLSI design that degrades the performance of any circuit. This brief proposed architecture an energy efficient multiplier in which the area, delay and power consumption are reduced to a great extent on comparing with the present works. The Vedic technology adopted in the multiplier makes the architecture even faster. The reduction of number of bits which takes part in multiplication reduces the complexity of the multiplication process and thus improves the efficiency. The m bit approximate vedic multiplier can be used for various digital signal processing applications where complex computations are to be performed.

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