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DC- LINK VOLTAGE UTILIZATION AND SWITCH FAULT DETECTION OF NPC INVERTER WITH SVPWM

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Abstract:

Now a day, efficiency is becoming an important role in power electronics. The technology leaders are focusing the inverter applications in the solar market, but also uninterruptible power supplies and motor drives have new targets for improving the efficiency.In Wind Turbine Generation (WTG) systems, a Neutral-Point-Clamped (NPC) topology is widely used because it has more compensations than a conventional two-level topology, particularly when operating at high power. The NPC topologyconsists of 12 switches in whichan open-switch fault in the NPC rectifier of the back-to-back converter leads distortion in the input current and also causes torque vibration in the system. To improve the reliability of Wind turbine system, an open-switch fault detection method for inverter using the NPC topology is required. This study analyzes effects of inner and outer open-switch faults of the NPC inverter and describes a novel open-switch fault detection and tolerance method for all possible open-switch faults inverter. The software makes it easy to deliver real-time output from the integrated circuit of the hardware. The Space Vector Pulse Width Modulation(SVPWM) is used for generating the pulse for switches whichshows good utilization of the DC-link voltage, low current ripple and is relatively easy to implement in the hardware, making it suitable for any high-voltage, high-power application.The simulation for the projected work is carried out throughMATLAB/SIMULINK.

Index Terms: Neutral point- clamped (NPC) topology, open switch fault detection and tolerance, space vector pulse width modulation (SVPWM), Wind Turbine Generating (WTG) System.

1. INTRODUCTION

BACK-TO-BACK power converters are widely used for power conversion in wind turbine generation (WTG) systems. Back-to-back power converters transfer power from a permanent-magnet synchronous generator (PMSG) to the grid. Back-to-back converters usually consist of two-leveltopologies;however, costly switching devices with high specifications(in terms of voltage and current)are needed in medium and high-power WTG systems.Multilevel topologies have the advantages of little current distortion and reduced collector-emitter voltage (VCE) [1].The grid- and machine-side topologies are the same and are known as the inverter andrectifier (according to the direction of power delivery).The demand for three-phase pulse width modulation (PWM) are connected to the grid through an L filter or an LCL filter.

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The Three-Level Neutral Point Clamped Multilevel Inverter is now becoming popular technology for medium voltage, high power applications like variable speed drives, power compensation and renewable energy applications due to its better quality of output voltage which involves the reduced harmonic distortion, lesser voltage stress across switches and it generates sinusoidal output waveform generation [3]. A neutral point clamped inverter is the most widely using inverter among all multilevel inverters [4]. Space Vector Pulse width Modulation (SVPWM) is used to generate the appropriate gate drive waveform for each PWM cycle.In our proposed system a three-level converter is used because it has low switching losses and superior output voltage quality [9].Normally, open switch fault is considered as line-line fault. In the load side output of three phases any one of phase is detected by fault it will by-passed through a thyristor switch. In our proposed system gate pulses for all the MOSFET switches is generated by using Space Vector modulation it will turn-on and turn-off the switches[5]. This paper is organized as several chapters:Wind turbine generating system, Back to Back converters,Neutral PointClamped Inverter topology, Space Vector Pulse Width Modulation and Open Switch fault detection and tolerance Methodology.

2. WIND TURBINEGENERATION SYSTEM

Wind energy conversion system is an important and popular renewable energy technology over other different renewable energy conversion technologies [1]-[3]. Wind energy capacity has grown rapidly over the last decade and has become the fastest grown renewable energy technology [2].Wind energy is produced by running wind turbine generator in a variable speed mode. According to the construction of the drive system, the turbines are classified into the geared and the direct drive type [3], [6]. The direct drive system has advantages such as lower cost, smaller size, and weight reduction [7]. Direct drive system like PMSG has many competitive advantages over other direct drive system because of its great energy yield, noise reduction, good reliability and high efficiency [6], [7].The controlled rectifier gives the bidirectional power flow capability, which is not possible in the diode rectifier based power conditioning system. Moreover, the controlled rectifier strongly reduces the input current harmonics and harmonic losses[8]. The grid side converter enables to control the active and reactive power flow to the grid and keeps the DC-link voltage constant and improving the output power quality by reducing total harmonic distortion (THD) [9]. The generator side converter works as a driver, controlling the magnetization demand and the desired rotor speed of the generator. A simulation analysis of back to back converter based wind turbine generator system was carried [1]. Due to some special features this converter topology has received great attention recently. New control techniques were proposed to improve the performance of inverter section [3], [4] and field programmable gate array (FPGA) based reconfigurable control strategy has been proposed [5]. An integrated control strategy of back to back converter has been developed for direct drive PMSG based wind turbine systems [2].

3. BACK-BACK CONVERTERS

The converter studied in this project is a Neutral-Point-Clamped three-level converter with three bridge legs[4]. “Three-level” means that each bridge leg, A, B and C can have three different voltage states. The converter topology can be seen in Figure 1 Switch 1 and 3 on each leg are complementary, which means that when switch 1 is on, switch 3 is off and vice versa. Switch 2 and 4 is the other complementary switching pair.

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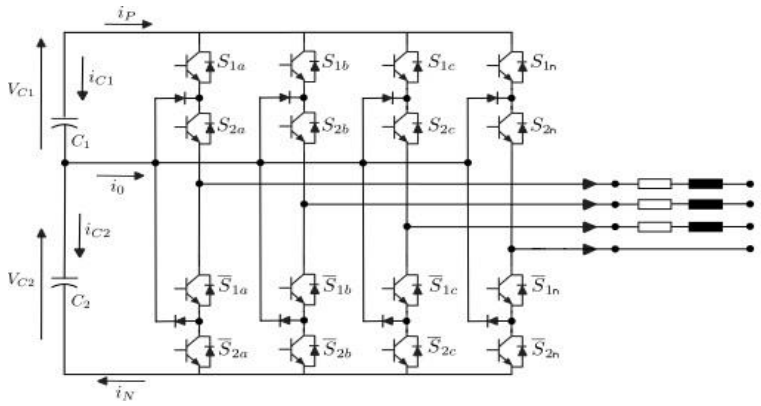

Fig:1 Back to Back Converter using Six Leg

If each of the capacitors has a constant voltage of 0.5 U_{dc}, then having the two upper switches on will give an output voltage of U_{dc}compared to level 0, switch 2 and 3 on will give 0.5 U_{dc} and by having the two lower switches on, an output voltage of 0 will occur. In addition to these three states there is a forbidden state where the first switch is on while the second is off.

Leg State	U_{a0}	T_{a1}	T_{a2}	T_{a3}	T_{a4}
2	U_{dc}	ON	ON	OFF	OFF
1	$0.5U_{dc}$	OFF	ON	ON	OFF
0	0	OFF	OFF	ON	ON

Table.1. Switching Operation OF back to back converter

The combination of states for the bridge legs give the space vectors plotted in table1 Space vector 210 means that bridgeleg A is in state 2, leg B in state 1 and leg C in state 0. Some of the switching states give the same space vector as is seenfor the inner vectors. All the modulation strategies discussed in the subsequent chapters use combinations of these switching states. The difference between the modulation strategies is the combinations of states and their respective extent.

4. NEUTRAL POINT CLAMPED INVERTER OPERATION WITH PMSG

Multilevel converter technologies have been increased in high-voltage and high-power applications [11]. Several kinds of topologies have been proposed such as diode- clamped (neutral-point)[12]-[13], capacitor-clamped (flying capacitors) [14]-[15] and cascaded multi-cell with separate DC source (isolated H-bridge) [16].The voltage difference ΔV between the input voltage provided by the NPC rectifier and the back electromotive force (EMF) of the PMSG generates the input current, which has a different phase angle from the voltage difference ΔV because of the inductance and resistance of the PMSG. The magnitude of the input voltage is almost the same as (or smaller than) the back EMF. If the two voltage magnitudes are almost the same, the current magnitude is determined by the phase angle difference between the input voltage and the back EMF. Zero current means that the two voltages are the

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same and that the phase angle of the input voltage matches that of the back EMF. For a unity power factor, the input voltage is

	NPC Topology	
Operating mode	Inverter	Rectifier
Current paths	Fig.2(b),(c),(d)and(e)	Fig.2(a),(b),(e)and(f)

Table.2. Operation Current Paths For Inverter/ Rectifier

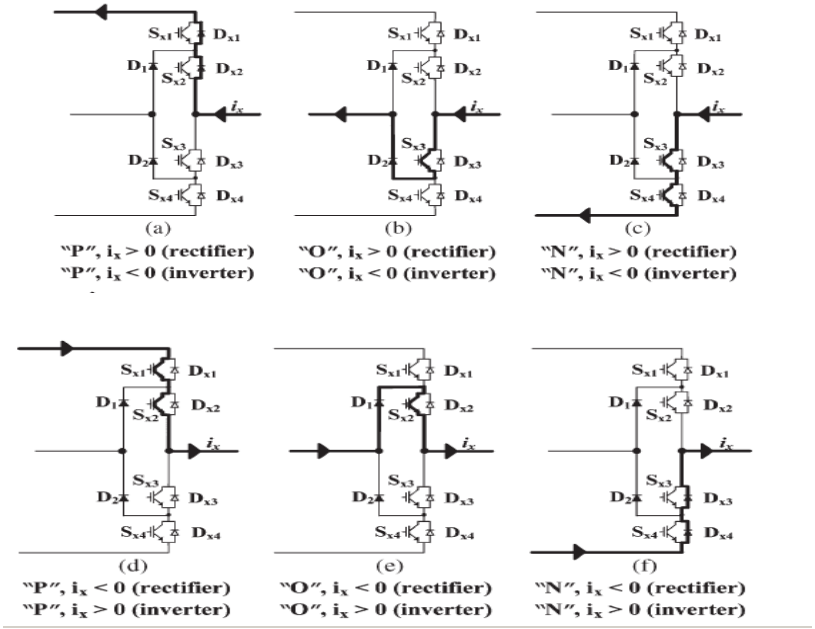

Fig.2 Rectifier and Inverter mode of operation

5. NEUTRAL POINT CLAMPED INVERTER

This diagram shows back-to-back power converters using a neutral-point-clamped (NPC) topology. There are three switching states for the three-level topology [19]. The first state is called "P" and refers to the state in which Sx1 and Sx2 are ON and Sx3 and Sx4 are OFF. When Sx2 and Sx3 are ON and when Sx1 and Sx4 are OFF, the switching state is referred to as "O." Switching state "N" means that Sx1 and Sx2 are OFF and Sx3 and Sx4 are ON. Consequently, most of the current in the inverter flows through the MOSFETs, and the currents through the freewheeling diodes are small.

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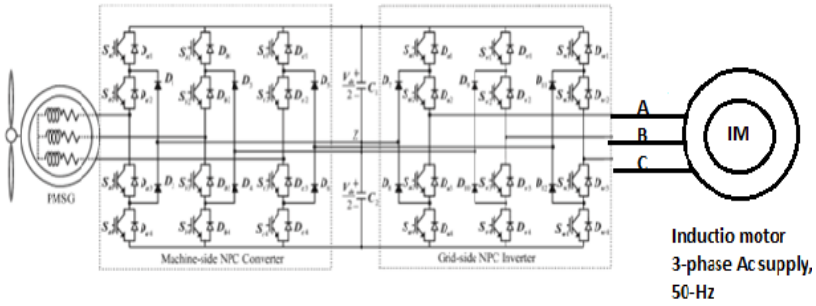

Fig: 3 Back-to-Back Converter using the NPC topology for the WTG system.

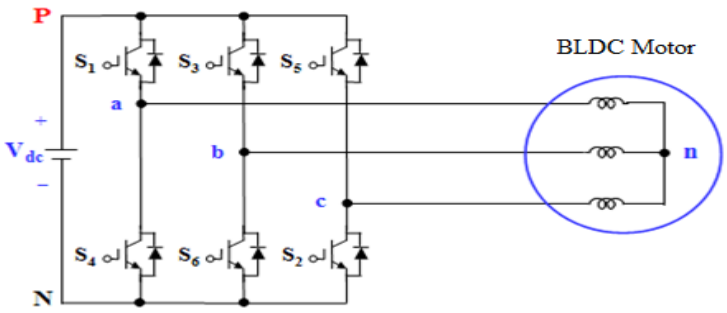

Fig3.1Three-Phase Voltage Source Inverter.

For the 180° mode VSI, each MOSFET conducts for 180° of a cycle. Like a 180° mode, 120° mode inverter also requires six steps, each of 60° duration, for completing one cycle of the output ac voltage. As seen in the Fig (3.2) the MOSFETs S1, S4; S3, S6 and S5, S2 are turned on with a time interval of 180 degrees. It means that S1 conducts for 180° of a cycle. MOSFETs in the upper group, i.e. S1, S3, S5 conduct at an interval of 120°.

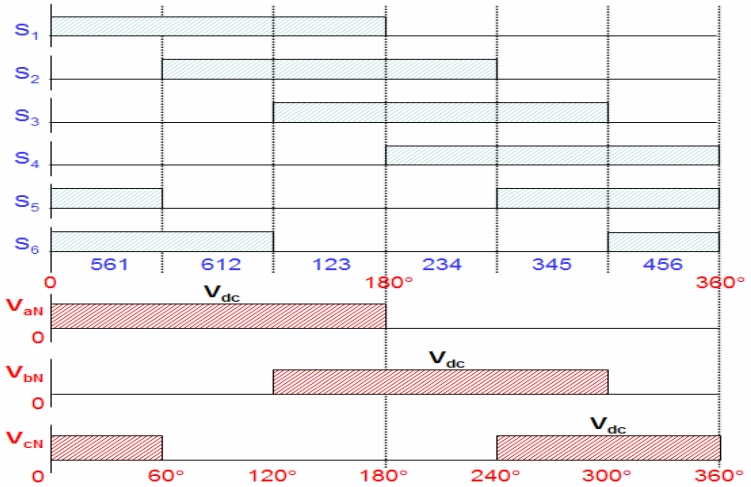

Fig3.2 Waveforms of Gating Signals, Switching Sequence, Line to Negative

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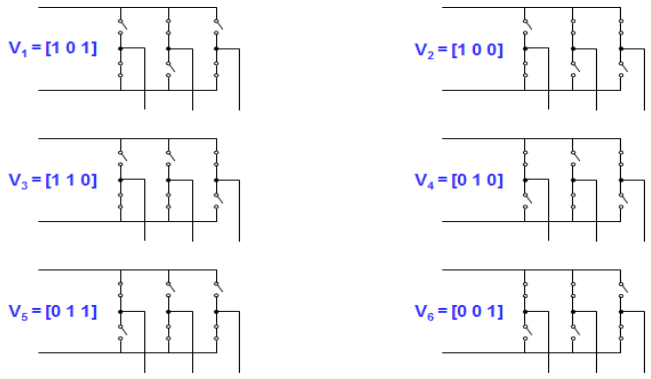

Fig:3.3 Switching Sequence For the Six Step VSI

As shown in the Fig.3.3 the switching sequence for the six step voltage source inverter is shown and the sequence is: 561 (V_1) → 612 (V_2) → 123 (V_3) → 234 (V_4) → 345 (V_5) → 456 (V_6) → 561 (V_1),Where, 561 means that S5, S6 and S1 are switched on similarly the other sequences.

The phase voltages are given as:

Van = $\frac{2}{3}V_{aN} - \frac{1}{3}V_{bN} - \frac{1}{3}V_{cN}$ ..... (1)

$$V_{bn} = -\frac{1}{3}V_{aN} + \frac{2}{3}V_{bN} - \frac{1}{3}V_{cN} \text{ ..... (2)}$$

$$V_{cn} = -\frac{1}{3}V_{aN} - \frac{1}{3}V_{bn} + \frac{2}{3}V_{cN} \text{ ..... (3)}$$

This is the proposed system block diagram of Dc Link voltage utilization and switch fault detection of SVPWM technique. In this Electric energy is obtained from renewable power conversion system like WTG it is given to rectifier and then to the inverter system. Any imbalance in voltage such as Over voltage, Under voltage that can be sensed by a voltage/signal conditioner the output signal is given to microcontroller by generating SVPWM pulse. Gate driver circuit is added for isolating and amplifying the signals. Therefore by using tolerance switch (Thyristor Switch) fault can be identified and tolerated.

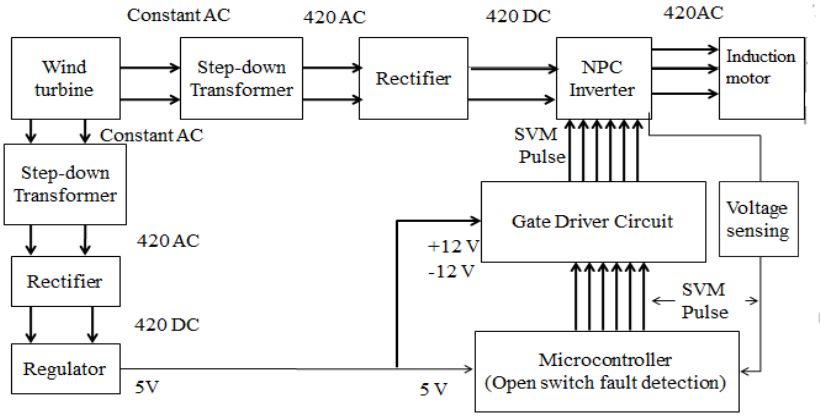

Fig .4. proposed system block diagram of NPC topology

International Journal of Global Engineering (IJGE) E- ISSN: 2456-3099
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6. SPACE VECTOR PULSE WIDTH MODULATION FOR MULTILEVEL CONVERTER

Space Vector Pulse width Modulation (SVPWM) generates the appropriate gate drive waveform for each PWM cycle. The inverter is treated as one single unit and can combine different switching states (number of switching states depends on levels). The SVPWM provides unique switching time calculations for each of these states [5]. This technique can easily be changed to higher levels and works with all kinds of multilevel inverters (cascaded, capacitor clamped, diode clamped). This can be described with the formula:

$$V= (T_1V_1+T_2V_2+T_3V_3)/T_c$$

SVPWM also have good utilization of the DC link voltage, low current ripple and relative easy hardware implementation. Compared to the SPWM, the SVPWM has a 15% higher utilization ratio of the voltage [17]. This feature makes it suitable for high voltage high power applications, such as renewable power generation. As the number of level increase the redundant switching states increases and also the complexity of selection of the switching states [1]-[11]. The below diagram 5shows a three-level neutral point clamped inverter. It contains 12 switching devices and also supplied with two capacitors connected in series [11]. Both are charged with VDC. The point between these capacitors is the DC-voltage neutral point. Each phase leg consists of 4 series-connected switching devices (MOSFET's) and two clamping diodes. Specific combinations of the twelve switches give the three- level output voltage.

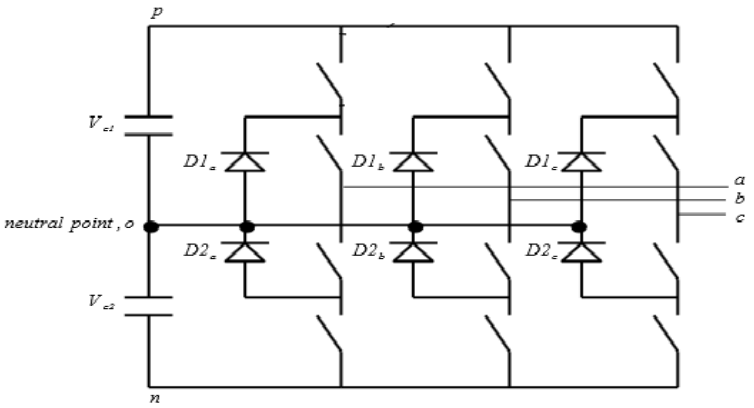

Fig.5 A three-level, three-phase neutral point clamped inverter

A. Switching States

For a three-level three-phase inverter there are 27 switching states. These states represent the connection to the different DC-link points. If there is a load connected to the output of these states the inverter will generate a output phase voltage.

This can be calculated as follows:

$$V_{a0} = (2S_{1a} - S_{1b} - S_{1c}) + (2S_{2a} - S_{2b} - S_{2c})$$
$$V_{b0} = (2S_{1b} - S_{1a} - S_{1c}) + (2S_{2b} - S_{2a} - S_{2c})$$

These are the line-to-neutral voltages. To receive the line-to-line voltage:

Vab=V a0−V b0 Vbc=Vb0−Vc0 Vca=V c0−Va0

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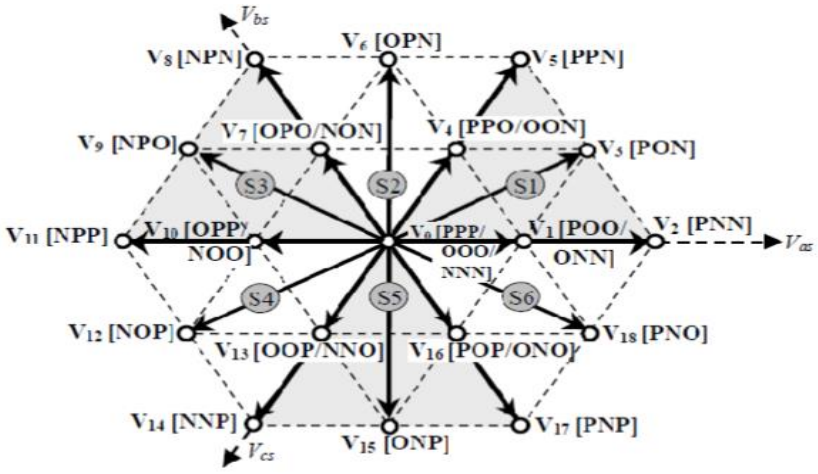

Fig5.1 Space vector diagram for a three-level inverter demonstrating 19 voltage vectors and 27 switching states.

A. Time duration

To describe the reference voltage vector Vref, the space vector transformations comes in handy:

$$V_{ref}=\frac{2}{3}(V_{a0}+V_{b0}.e^{j\frac{2}{3}\pi}+V_{c0}.e^{-j\frac{2}{3}\pi})$$

$$V_{ref}=V.e^{j(\omega_0 t-\gamma_0)}=\mathrm{V}<\Theta_0$$

V_{ref} can be described with the three nearest voltage space vectors. This selection is based on the magnitude of the Vref and its angle. For one cycle:

$$V_{ref}=T_1V_x+T_2V_y+T_3V_z$$

If V_2 is chosen as the reference axis (maximum magnitude as units) the voltage vectors on the axis can be described as:

$$V_x=V_1=\frac{1}{2},V_y=V_3=\frac{\sqrt{3}}{2}.e^{j\frac{\pi}{6}},V_z=V_4=\frac{1}{2}.e^{j\frac{\pi}{3}}$$

and the reference vector as:

$$V_{ref}=V_u.e^{j\Theta}$$

Where, $V_u=\frac{V}{\frac{4}{3}V_{DC}}$

V_{ref} Informs of the real and imaginary axis:

$$V_u=(\cos(\Theta)+jsin(\Theta))=\frac{1}{2}T_1+\frac{\sqrt{3}}{2}\left[\cos\left(\frac{\pi}{6}\right)+jsin\left(\frac{\pi}{6}\right)\right]T_2+\frac{1}{2}[\cos\left(\frac{\pi}{3}\right)+jsin\left(\frac{\pi}{3}\right)]T_3$$

Dividing the formula in real and imaginary part eases the calculations for the duty cycles:

$$\text{Real part:}\frac{1}{2}T_1+\frac{\sqrt{3}}{2}\cos\left(\frac{\pi}{6}\right)T_2+\frac{1}{2}\cos\left(\frac{\pi}{3}\right)T_3=V_u.\cos(\Theta)$$

$$\text{Imaginary part:}\frac{\sqrt{3}}{2}sin\left(\frac{\pi}{6}\right)T_2+\frac{1}{2}\sin\left(\frac{\pi}{3}\right)T_3=V_4.\sin(\Theta)$$

The duty cycles is then given in form of:

International Journal of Global Engineering (IJGE) E- ISSN: 2456-3099
VOL 1 ISSUE 3 (2017) PAGES 56 - 72
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$$T_1 = 1 - 2(\frac{2V_u}{\sqrt{3}}) \sin(\Theta) = 1\text{-}2.a.\sin(\Theta)$$

$$T_2 = 2.a.\sin\left(\Theta + \frac{\pi}{3}\right) - 1$$

$$T_3 = 2.a.\sin\left(\Theta - \frac{\pi}{3}\right) + 1$$

The duration time for the vectors will give information about the duty cycle for each switch.

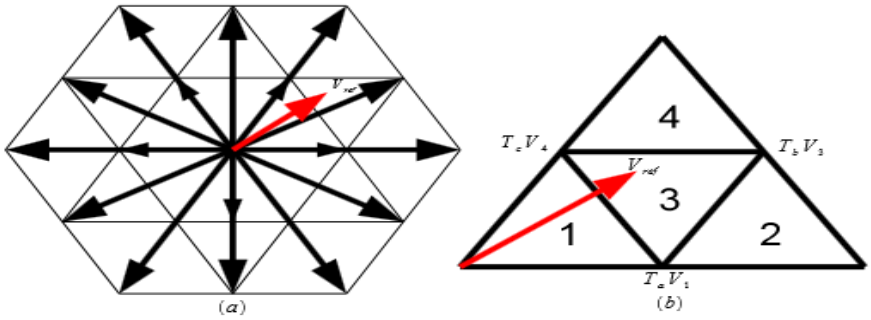

Fig. 5.2 Space vector diagram for (a) all sectors (b) sector 1

7. FAULT-TOLERANT CONTROL IN WIND ENERGY CONVERSION

Figure 6showsthe proposed fault-tolerant wind energy conversion system (WECS) topology, which is based on a classical back-to-back converter and uses common redundant legs for the GSC. The proposed fault-tolerant system is composed of three different units which are the phase isolation unit, phase reconnection unit, and additional leg unit[18]. The redundant legs consist of the switches S7, S8, S9, S10, S11, and S12, and are used to replace the faulty one of the other legs under any power switch failure in the GSC..During the normal operation, three Thyristor switches in the isolation unit are turned ON whereas three Thyristor switches in the reconnection unit are turned OFF.

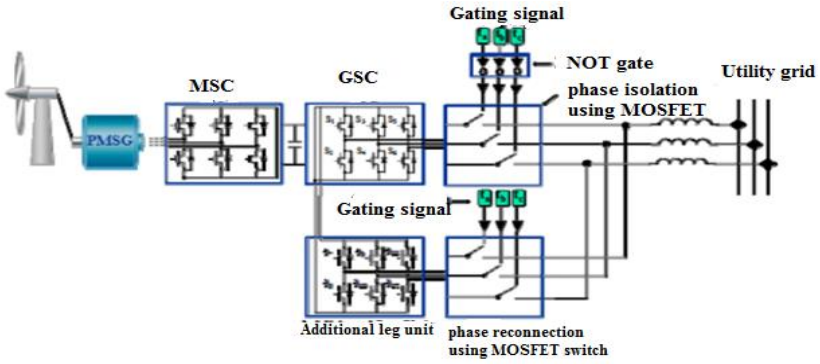

Fig.6. The proposed fault-tolerant wind energy conversion system (WECS)

Figure 6.1 shows the operation of the entire system during the normal healthy operation. During healthy operation, the additional leg unit will be inactive. By using the gating signal, the isolated faulty phase is replaced with the additional leg unit to allow continuous operation of the GSC.

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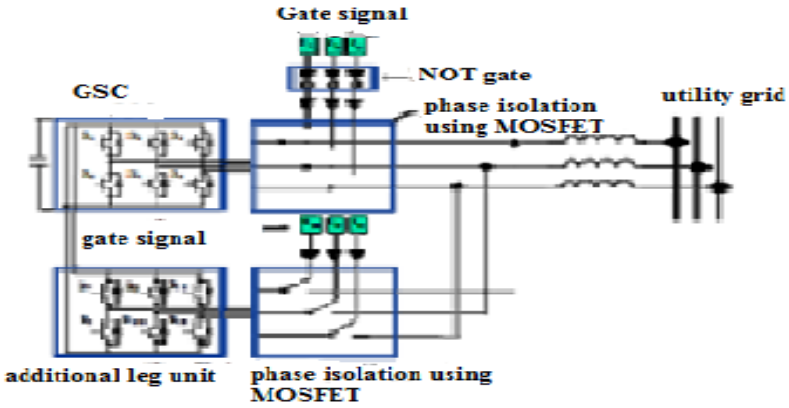

Fig.6.1 during normal operation condition of Switch

Figure 6.2 shows the fault-tolerant topology under the switch S1 open fault. As soon as the fault location is determined, a remedial strategy is performed to guarantee a continuity of operation[4]. In this case, a-phase Thyristor of the isolation unit is turned OFF and a-phase Thyristor of the reconnection unit is turned ON at the same time.

The fault-tolerant topology under the switches S1 and S3 open fault. Because the faults occur in a-phase and b-phase simultaneously, a-phase and b-phase Thyristor switches of the isolation unit are turned OFF and a-phase and b-phase Thyristor switches of the reconnection unit are turned ON. The gating signals of ta, tb, and tc are utilized to turn ON and OFF the Thyristor switches, if any open-switch fault occurs.

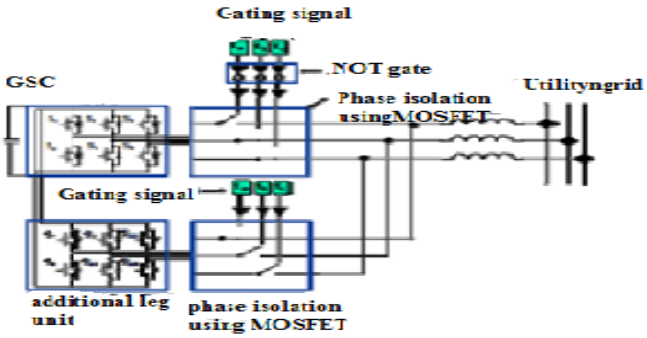

Fig.6.2 Fault tolerance methodologies

These gating signals are determined using the durations of corresponding phase current. During the normal operation, the values oft_a,$t_b$and t_c used for the gating signals are zero to turn ON the Thyristor switches in the isolation unit. Under the fault condition, on the contrary, these values are changed to one to turnOFF the Thyristor switches in the isolation unit and to turn ON the Thyristor switches in the reconnection unit simultaneously.

The phase of the current is not the same as the phase of the pole voltage, as mentioned in Section II. The Sx2 open switch fault prevents the “O” and “P” switching states from supplying a negative current The positive current becomes zero because the “O” switching state of the positive current isblocked Likewise, the distorted a-phase pole voltage in the interval of the blocked Consequently, the Sx2 and Sx3 open-switch faults in the rectifier significantly distortthe current and cause torque ripple in the PMSG.

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8. SIMULATION RESULTS

The simulation used to done this fault tolerance made in switches is MATLAB/SIMULINK.

A. Software Tools

MATLAB is a high-performance language for technical computing. It integrates computation, visualization, and programming in an easy-to-use environment whereproblems and solutions are expressed in familiar mathematical notation.

MATLAB is a high-level language and interactive environment that enables to perform computationally intensive tasks faster than with traditional programming languages such as C, C++, and FORTRAN.

B. Simulation Diagram

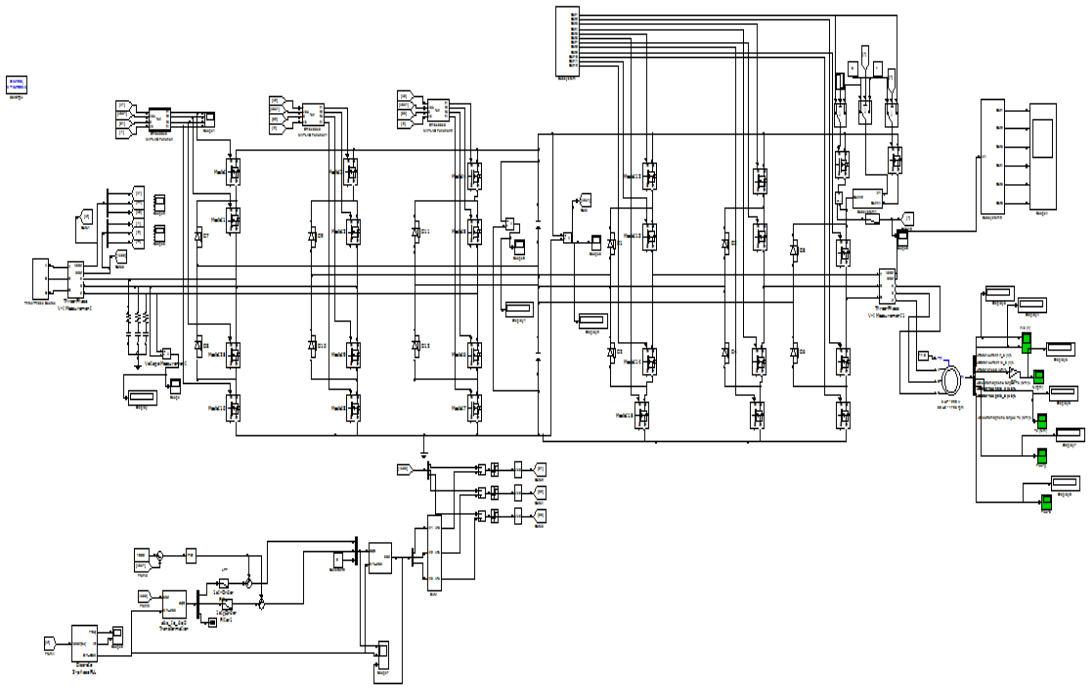
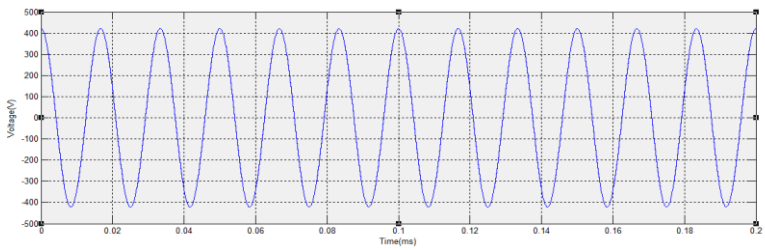


Fig.7. Open switches Fault Detection and Tolerance in the Induction motor.

C. SIMULATION OUTPUT RESULTS



International Journal of Global Engineering (IJGE) E- ISSN: 2456-3099
VOL 1 ISSUE 3 (2017) PAGES 56 - 72
Received: 01-03-2017. Published: 17-03-2017

Fig.8. Rectifier Input

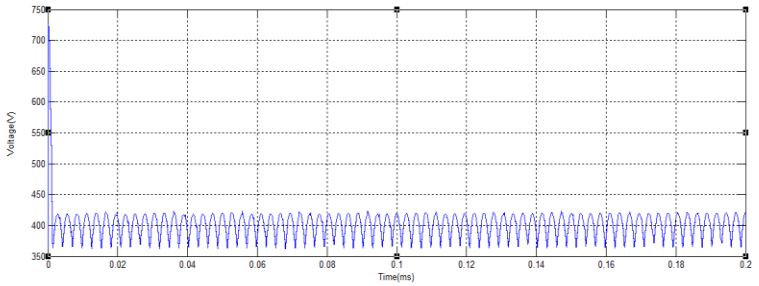


Fig.9. Rectifier output

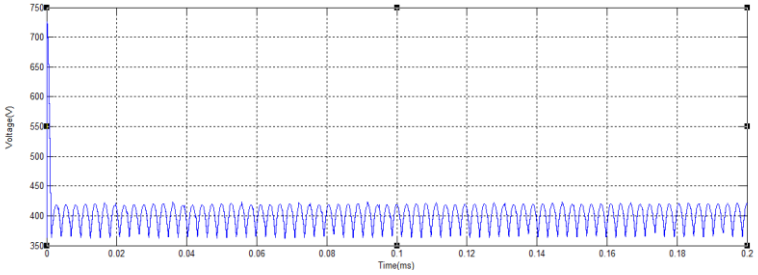


Fig.10. Inverter Input

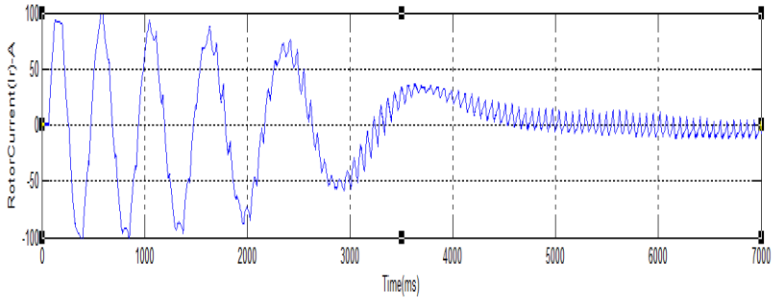


Fig.11. Rotor Current

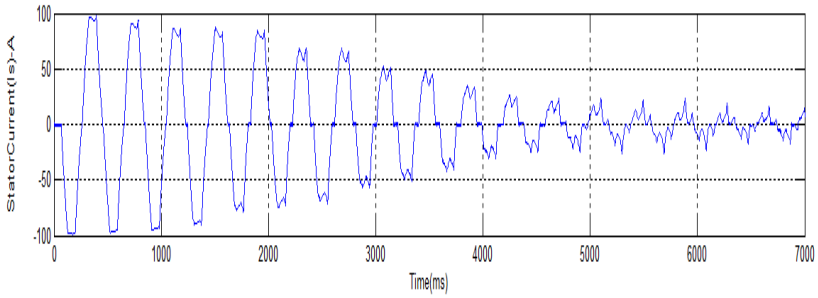


Fig.12 Stator Current

International Journal of Global Engineering (IJGE) E- ISSN: 2456-3099
VOL 1 ISSUE 3 (2017) PAGES 56 - 72
Received: 01-03-2017. Published: 17-03-2017

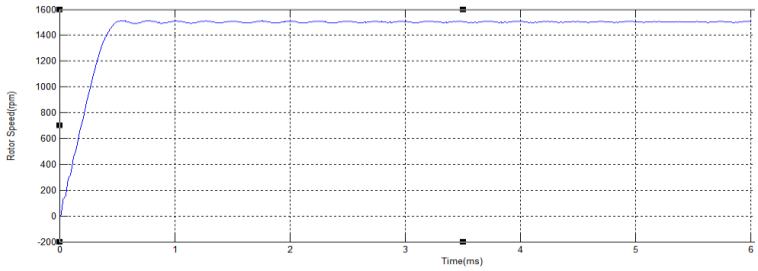


Fig.13 Rotor Speed

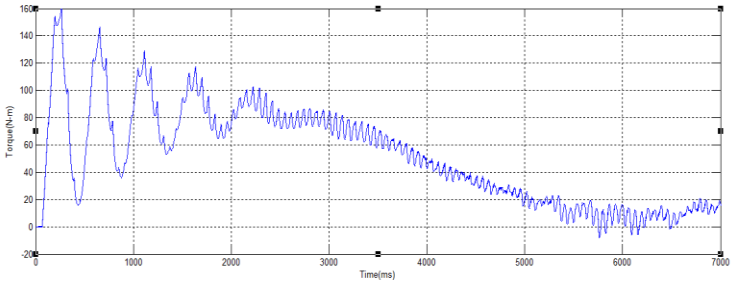


Fig.14 Electromagnetic Torque

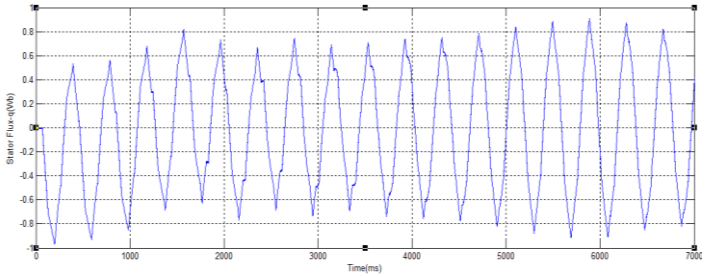


Fig.15 Stator Flux-q axis

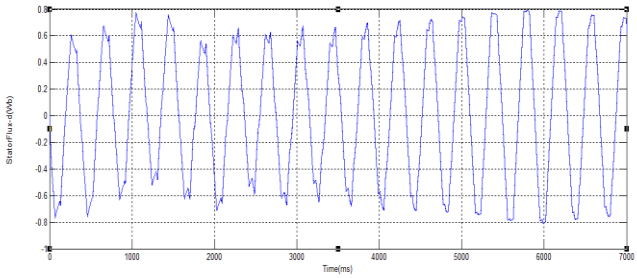


Fig.16 Stator Flux-d axis

TABLE 3 INPUT ANALYSES

INPUT RMS VOLTAGE	RECTIFIER INPUT	RECTIFIER OUTPUT	INVERTER INPUT
415V(3-PHASE AC VOLTAGE),50HZ	421.4V	421.3V	421.3V

International Journal of Global Engineering (IJGE) E- ISSN: 2456-3099
VOL 1 ISSUE 3 (2017) PAGES 56 - 72
Received: 01-03-2017. Published: 17-03-2017

TABLE.4 WITHOUT USING TOLERANCE SWITCH- OUPUT ANALYSES

FAULT TYPE	STATOR CURRENT(Is)	ROTOR CURRENT(Ir)	ROTOR SPEED(Nr)	ELECTROMAGNETIC TORQUE	STATOR FLUX(q)	STATOR FLUX(d)
PHASE-GROUND FAULT	-5.811A	-5.811A	1505rpm	13.51N-m	0.8407Wb	0.03691Wb
PHASE-PHASE FAULT	-4.832A	-4.832A	1501rpm	14.64N-m	0.8458Wb	0.0424Wb

TABLE 5. WITH USING TOLERANCE SWITCH- OUPUT ANALYSES

FAULT TYPE	STATOR CURRENT(Is)	ROTOR CURRENT(Ir)	ROTOR SPEED(Nr)	ELECTROMAGNETIC TORQUE	STATOR FLUX(q)	STATOR FLUX(d)
PHASE-GROUND FAULT	17.84A	-6.988A	1499rpm	16.43N-m	0.8251Wb	0.05641Wb
PHASE-PHASE FAULT	19.37A	-8.297A	1502rpm	12.91N-m	0.8578Wb	0.03299Wb

9. HARDWARE DETAILS

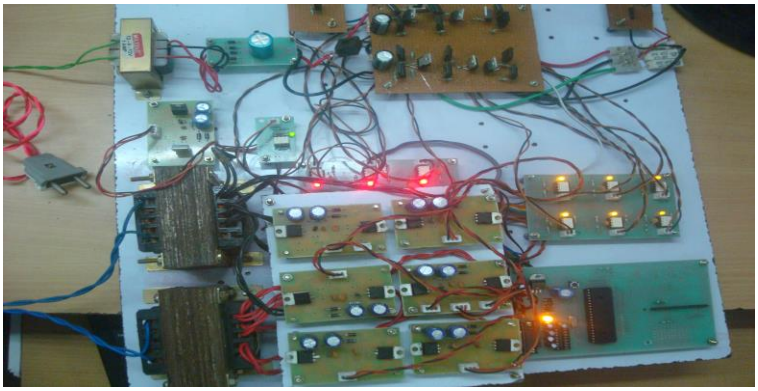


Fig.17 diagram of hardware kit

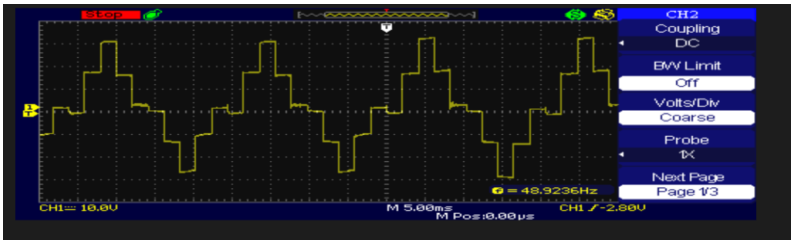


Fig.18 waveform of switches at normal condition

International Journal of Global Engineering (IJGE) E- ISSN: 2456-3099
VOL 1 ISSUE 3 (2017) PAGES 56 - 72
Received: 01-03-2017. Published: 17-03-2017

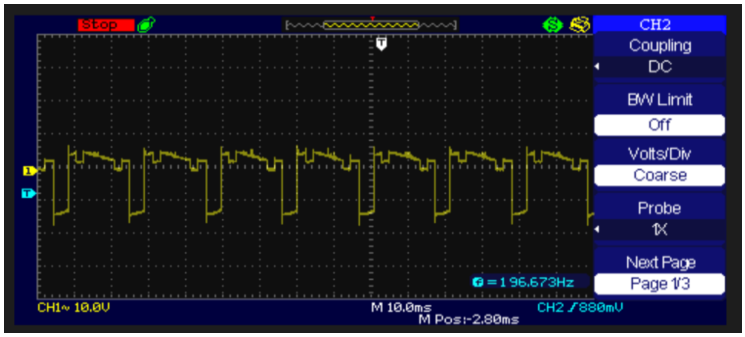


Fig.19 waveform of switches at faulty condition

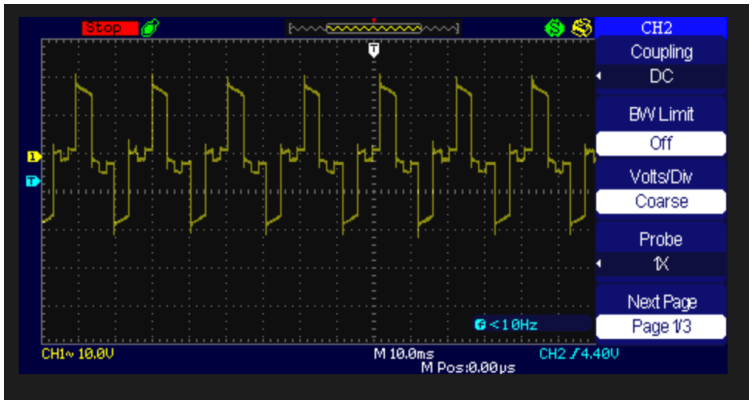


Fig.20 phase to phase waveform at fault condition

This diagram shows when switch at fault condition that faultis tolerated by using another tolerancing switch .

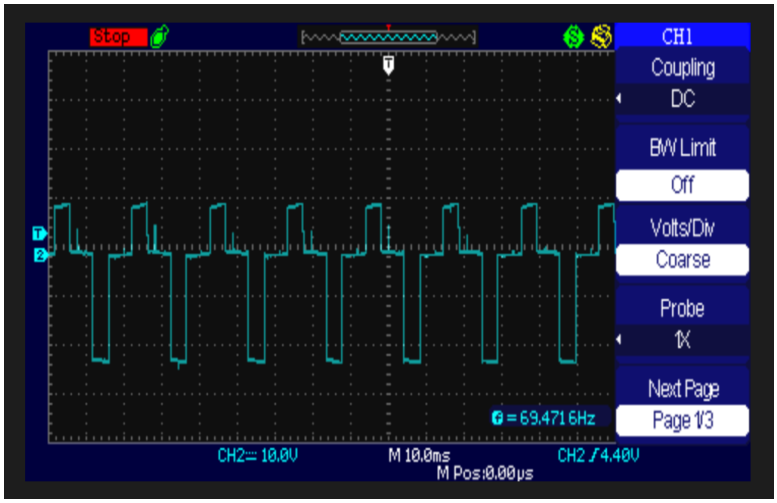


Fig.21waveform of phase to neutral fault tolerance

International Journal of Global Engineering (IJGE) E- ISSN: 2456-3099
VOL 1 ISSUE 3 (2017) PAGES 56 - 72
Received: 01-03-2017. Published: 17-03-2017

CONCLUSION

An open switch fault detection and tolerance method using Neutral Point Clamped inverter with Space Vector Pulse Modulation has been proposed in this paper. The proposed method just uses thyristor switch for tolerating the fault occurring in the one or two switches simultaneously. To identify the location of fault SVPWM technique has been used. It is the advanced method of generating pulses then conventional PWM and SPWM. Moreover, the performance of the proposed system was confirmed for Resistive load and Resistive Inductive load also. Fault bypassing through a switch has become done within nanoseconds. So, the efficiency of the system is increased. This proposed system has better efficient for DC-link voltage utilization and low current ripple factor. Consequently the proposed open switch fault detection and tolerance is advantageous is that it does not require additional devices and uses calculations.

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