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DUAL FREQUENCY PHASE SHIFTED CARRIER PWM BASED SINGLE PHASE CASCADED MULTI LEVEL CONVERTER FOR ENERGY STORAGE SYSTEM

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ABSTRACT:

Cascaded multilevel converter (CMC)-based energy storage system, which consists of cascaded H-bridge converters and energy storage components, is a promising option to compensate fluctuating electric power of renewable energy. This project proposes a novel single phase CMC-based battery storage system, which includes an LC branch. The cascaded converter cells and the LC branch form an auxiliary power loop, which could realize active power exchange between different cells with the proposed dual-frequency phase-shifted carrier pulse width modulation (DFPSC PWM). The principle and effectiveness of DF-PSC PWM and the power transfer mechanism are analyzed. Meanwhile, the design of the tuned filter, output filter, and the state of charge balancing control system is introduced. The operation principle of the power exchange in the proposed energy storage system can be verified by simulation and experimental results.

Index Terms: Auxiliary power loop, cascaded multilevel converter (CMC), energy storage system (ESS), power exchange.

1. INTRODUCTION

The cascaded multilevel converter (CMC) is a promising solution to obtain high voltage from low-voltage devices. Since switching is between several smaller voltage levels, the CMC has lower dV/dt than two-level converters. Meanwhile, its modular structure allows the usage of low-cost switching devices with low electromagnetic interference, low total harmonic distribution at low frequency and high fault-tolerance capability. For this reason, CMC has been widely employed in high-power applications such as static synchronous compensator (STATCOM) and motor drivers. In recent years, its prominent structure makes it suitable for single-phase energy storage applications ,which require obtaining high voltage from low-voltage devices, i.e., traction converter in HV with battery, regenerative breaking with EDLC. Compared to the traditional transformer-based multi pulse converters, CMC reduces the voltages of individual energy storage unit. More over, high energy efficiency is achieved via its transformerless single-stage circuit structure.

The use of CMC in these applications is considered to be a good tradeoff in between complexity and reliability. Although the number of active switches and control complexity will increase, topology and redundancy allow CMC-based converters to achieve more than one goal within the imposed control system. For example, the dc-link balancing control can be realized without extra circuits. In most CMC applications, the dc-link balancing is fundamental for the safe operation of the system. For CMC-based STATCOMs, adequate methods for maintaining the balance of the capacitor voltages have been employed in the literature [10], [11]. For the CMC-based energy storage system (ESS), the internal impedance and the self-discharge rate are different in each energy storage component, i.e., battery cell or EDLC cell, because of the

manufacturing discordances. In a series-connected configuration, the difference of parameter between cells will result in unbalanced voltage/state of charge (SOC). The unbalance of voltage/SOC could reduce the performance of the ESS since some of the cells cannot provide the expected active power while others can. This situation could cause the destruction of the individual energy storage component, and even the failure of the whole system. There have been some balancing circuits for series connected battery/EDLC packs, which can be classified as passive balancing circuit and active balancing circuits. The active balancing circuits could effectively equalize the SOC/voltage within series-connected battery/EDLC by transferring energy from cells to cells with dc–dc converters. However, an additional balancing circuit not only increases system complexity but also reduces efficiency. Thus, dc-link balancing control strategies without additional active circuits have been proposed in the literature for a CMC-based system. The voltage balancing methods of single-phase CMC battery energy storage system (BESS) based on staircase modulation have been introduced. The main idea is to sort the batteries according to their voltage. By controlling the switch angles, the discharging rate of the battery with highest voltage is higher than others. However, these methods are only effective for staircase modulation. Meanwhile the voltage balancing speed depends on the load current and cannot be adjusted. The ideas of injecting zero-sequence voltage or negative-sequence current into the three-phase system for dc-link balance are introduced. These injected components affect the individual branch powers but keep the total three-phase power transfer unaffected. However, the maximum tolerated voltage variation and semiconductor current rating restrict the injected voltage/current as well as the balancing power. The magnitudes of carrier waves are updated in each ac voltage cycle to change the output voltage of H-bridges. The battery with the highest SOC will discharge at highest rate to diminish the SOC unbalance.

However ,the differences between carrier wave magnitudes should be limited in certain level to avoid unexpected output voltage levels. Generally speaking most existing approaches for dc-link balancing use small shifts of the switching patterns to adjust active power of each energy storage cells . Since the adjust range is usually limited, the dc-link balancing period is unexpected and the effectiveness depends on the magnitude of the converter current. In addition, design and implementation of multiple balancing control loops are difficult, especially when these are coupled with the fundamental modulators. Consideringpracticalapplicationrequiresfastbalancingduringtransient disturbances, a balancing control strategy with extra degree of freedoms and independent power control capability is needed. In a distinct dc-link capacitor voltage control strategy for CMC-based STATCOM is proposed. By injecting orthogonal voltage components, direct control of the balancing current and power are achieved. However, since the fundamental and balancing power flow in the same loop, the output voltage variation of H-bridges is inevitable. Inspired by this idea, a novel active power exchange control strategy is proposed in this paper. By introducing an auxiliary power loop into the CMC and injecting the secondary frequency voltages, a particular H-bridge could generate active power at one frequency and absorb it at another. Thus, the charge/discharge mode of energy storage components in different H-bridges can be controlled individually. With the proposed topology and control strategy, the energy can be directly transferred from one battery to another, from one EDLC cell to another even when the CMC is standby. Since the auxiliary power loop is independent from the fundamental one, the power transfer can be controlled in a relative large range. This paper is organized as follows: After Section I, a CMC with an auxiliary power loop is proposed in Section II. This converter uses segmented energy storage components as dc source. The dual-frequency phase-shifted carrier pulse width modulation (DF-PSC PWM) used in the proposed system is carefully analyzed. In Section III, the design of tuned filter and output filters is discussed.

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2. SYSTEM STRUCTURE AND POWER EXCHANGE PRINCIPLE

A. System Description

The proposed single-phase CMC-based ESS is shown in Fig. 1. The CMC includes n series-connected H-bridges and n energy storage components. An LC branch is paralleled with the cascaded H-bridges, which consists of Lr ,C r, and Rr. The LC branch is tuned at resonant frequency fn. In CMC-based ESS, assignment of n is a trade off among cost,power quality, and control complexity.

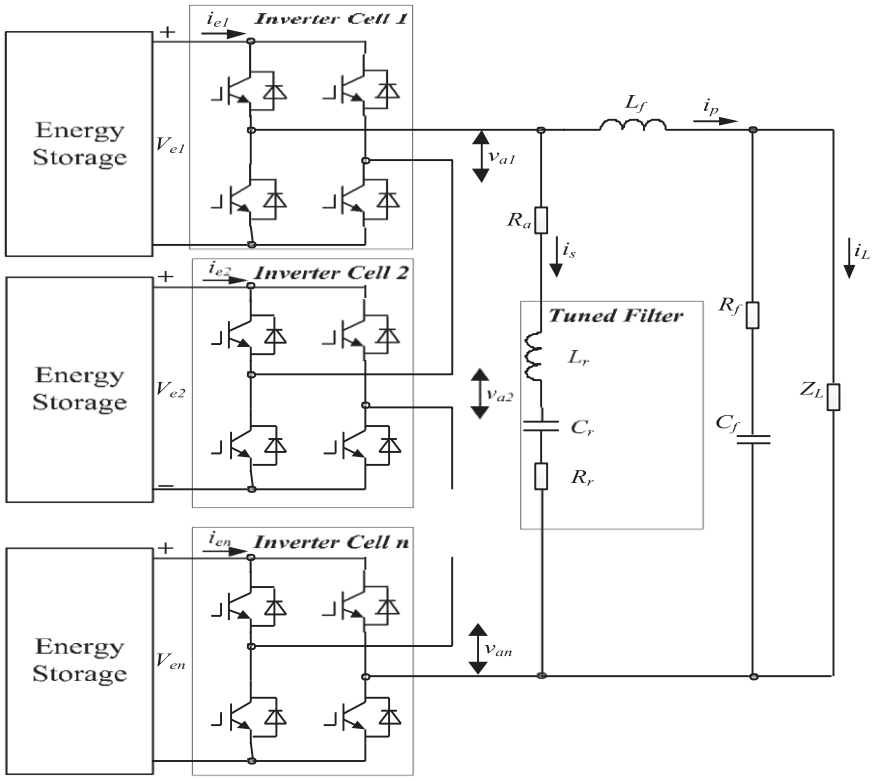

Fig. 1.Topology of proposed CMC with auxiliary power loop

B. Principle of DF-PSC PWM

The main advantage of the proposed cascaded ESS is that the power exchange control between energy storage components and the active power control of the ESS are decoupled with each other. The DF-PSC PWM modulation method is adopted to generate gate signals of switches in H-bridges.

Since two different frequency components are combined in DF-PSC, the intersections of reference and carrier wave form are different from the traditional PWM. Thus, the existing mathematic conclusions of PWM voltage waveforms cannot be used to analyze the DF-PSC output voltage. In this section, the mathematical model of DF-PSC is derived and voltage components at different frequencies are achieved.

C. Power Exchange Control Methods Analysis

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If Mi (i = 1 ,2,3)are identical, the active power produced by current and voltage at fundamental frequency of the CMC is equal to Pm, which is delivered to the load. Based on the orthogonal power flow theory, we can analyze the power produced by current and voltage at auxiliary frequency independently. In power exchange application, we assume that the energy in E1 need to be transferred to E3. Thus, in auxiliary power loop, E1 needsbein“discharging”state,E3 in“charging”state,andE2 in “standby” state, i.e., there is no active power exchange between E2 and the other two components. The quotation marks imply that these operation states are defined in auxiliary power loop. E1–E3 are actually all in discharging state in the fundamental power loop.

A phase-shifted power exchange control method is proposed to manipulate the operation states of E1–E3 in auxiliary power loop. In order to simplify the analysis of the converter, the following assumptions are made:

1) The dc voltages of all energy storage components are constant Vc;
2) Current flow at auxiliary frequency is kept in the auxiliary power loop;
3) the equivalent impedance of the series *LC* branch at *fa* is pure resistance ($Z(j\omega a) = Rr$);
4) all switches, diodes, inductor, and capacitor are ideal com- ponents.

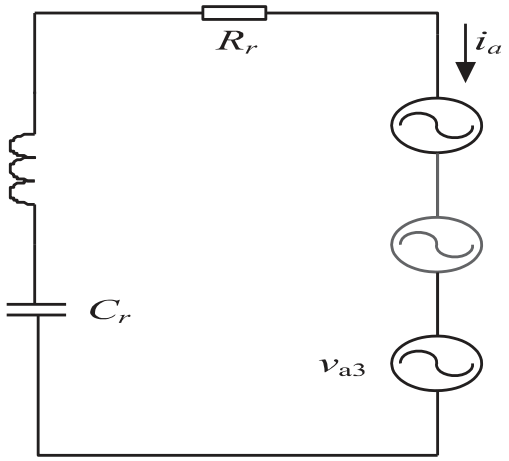

Fig.2. Equivalent circuit of auxiliary power loop.

3. CIRCUIT PARAMETER AND CONTROL SYSTEM DESIGN

A. Output Filter Design

The design of tuned filter and output filter is discussed in this section. The equivalent circuit with ac source and filters is shown in Fig. 7. The summations of output voltages at fundamental frequency (vm1 −vm3) and auxiliary frequency (va1 −va3) are simplified to equivalent ac sources vm and va. There is vs = vm + va. The tuned filter consists of Lr,C r, and Rr. Its objective is to generate a low-impedance path for the auxiliary frequency current ia. The output filter consists of Lf ,Cf, and Rf. Its objective is to guarantee the output power quality of the inverter. The filter resistor Rf is designed to result in an over damped circuit. Rf can be set equal to the characteristic impedance of the cable to absorb the reflected energy.

B. Tuned Filter Design

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The tuned filter has three passive components: resonant inductor Lr, resonant capacitor Cr, and resonant resistor Rr. The ideal relation between resonant capacitance and inductance in the tuned filter is

$$\omega aLr = 1/\omega aCr$$

where $\omega a = 2\pi fa$.

C. SOC Balancing Control

In CMC with integrated energy storage, unbalanced SOC values have a negative effect on the normal operation of the system. Although the proposed power exchange control method based on DF-PSC PWM could be used in various fields, we choose SOC balancing control as an example to illustrate the decoupled energy control loops. However, in this paper, we do not intend to explore such SOC balancing issues as optimized algorithm and balancing speed comparison. The SOC balancing control is used to verify the proposed power exchange theories.

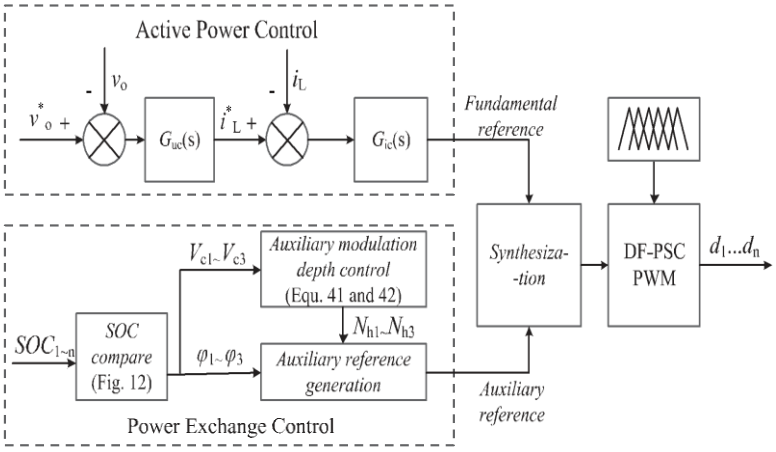

Fig.3.Construction Figure

4. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the proposed topologies and theoretical analysis, the model of a BESS with cascaded H-bridges and a tuned filter are simulated with MATLAB/SIMULINK simulation software. The detailed parameters are listed in Table II. The output waveforms of open-loop simulation with preset parameters are shown in Fig. 10, in which (a) shows the output voltage of the cascaded H-bridges vs, (b) shows the auxiliary current in the tuned filter io, and (c) shows the system output voltage of the vo.vs is seven-levels step waveform modulated with DF-PSC PWM. Because of the frequency effect of the tuned filter, ia is 500 Hz sinusoidal current. The system output voltage vo is 50 Hz sinusoidal wave since the output filter eliminates the auxiliary frequency component and the side bands harmonic components in vs. The peak output voltage is regulated at 50 V. That proves the effectiveness and independence of active power control.

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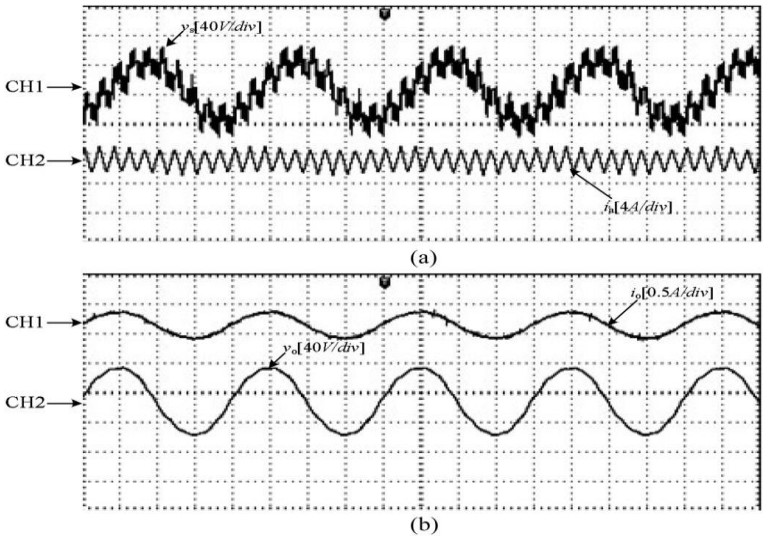

Fig.4. FFT analysis result of the output voltage and current. (a) output voltage vol (b) output current io .

CONCLUSION

A novel CMC-based ESS, which contains an auxiliary power loop to exchange power between H-bridges, is proposed in this paper. The auxiliary power loop is realized by introducing a se- ries *LC* branch into the CMC and applying the DF-PSC PWM. The mathematic analysis indicates that the voltages at funda- mental frequency and auxiliary frequency are independent to each other with DF-PSC PWM. By controlling the phase dif- ferences between the auxiliary frequency voltages, power could be transferred from one H-bridge to another. However, we face a tradeoff between transferred power and efficiency. In CMC based BESS, the proposed power exchange mechanism could be used for SOC balancing. Simulation and experimental results verify the operation principle of the converter.

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